NEXT GENERATION PHASE COHERENT INSTRUMENTATION RECEIVER

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ABSTRACT

The next generation of antennas will benefit from advanced instrumentation receivers capable of providing simultaneous analog and digital IF inputs, better TR pulse synchronization and high resolution pulse profiling. One such receiver uses a synergistic combination of a tightly coupled FPGA based beam controller, high performance analog digitizers, multiple FPGA based digital signal processors and a new mathematical programming environment. The FPGA signal processor provides direct digital downconversion, high resolution pulse processing and dynamically reconfigurable time and frequency gated matched filter signal integration. The signal processing functions are fully scriptable, providing spectral analysis, various other types of transform analysis, instantaneous demodulation, pulse characterization, noise estimation and more. Advanced mathematical tools combined with novel user interface technologies provide multiple intuitive views into the test setup, error analysis and measurement environment.

Keywords: instrumentation receiver, multibeam antenna measurements, TDMA, pulse measurements, user interface.

1. Introduction

Antennas are becoming complex and tightly integrated with RF and other system components. Emerging antenna test applications include active element phased arrays, antennas with digital IF outputs, frequency agile operation and active antennas using narrow pulse operation.

Figure 1 – Next generation Panther 9000 receiver

Figure 1 shows one version of the receiver. The phi display on the right provides an intuitive real time view of the measurements. This receiver can be controlled from a separate host computer or by a web browser.

2. NSI receiver development history

The new receiver design was strongly influenced by lessons learned from several earlier versions. All receivers were part of interferometer systems which provide complex (amplitude / phase) gain measurements relative to a reference path. The interferometers always include a RF source, a power splitter and two independent propagation paths, one of which includes the test article. The receiver then computes the complex gain ratio between the signal and reference paths.

The first generation receiver was an element of a simple swept frequency interferometer that was used for radar cross section (RCS) and inverse synthetic aperture radar (ISAR) measurements [1,2]. This early receiver used deceptively simple hardware to create an unusual form of a superheterodyne receiver. The receiver used a single mixer to produce real channel only data. Quadrature data was derived through the use of a software based Hilbert transformer. Although this receiver appeared to be a low performance homodyne zero IF design, it was in actuality, a high performance superheterodyne design. The poor performance of homodyne receivers is generally due to LO leakage and 1/f noise within the mixer. In this receiver, the RF sweep combined with an intentionally introduced interferometer path length unbalance shifts the IF away from DC, suppressing the LO leakage and reducing 1/f noise. A significant disadvantage of this receiver was the need for swept frequency operation.

The RCS / ISAR receiver was followed by the development of a phase modulated interferometer (PMI) [1,3]. The PMI provided the advantage of fast frequency agile CW complex gain measurements without the swept frequency requirement of the earlier receiver. The PMI internally included a fast tuning local oscillator (LO) that used a linearly swept phase modulator. This design is analogous to an ECM serrodyne modulator and is a form of a direct digital frequency synthesizer. A broad band 2 to 26 GHz phase modulator was used in the PMI to introduce a single side band (SSB) carrier frequency shift to the transmit path. The unaltered carrier signal was used as the receiver mixer LO source. The mixer output was at

the serrodyne IF frequency and was digitally processed to produce the complex gain measurements. The LO phase modulator had frequency dependent gain and phase circularity errors which were identified by comparison to a Hilbert transformer. Although this receiver was fast and frequency agile, it suffered from spurious harmonic content and amplitude modulation in the transmit path, from the need for RF frequency dependent circularity correction and a 2 to 26 GHz operational frequency range limitation.

The PMI receiver was followed by the Panther 6000 series instrumentation receivers [4]. Like the previous receivers, this receiver was heavily based on digital signal processing. The receiver digitized a pair of 20 MHz IF signals which were then digitally downconverted to a baseband signal. The digital downconverter operated by forming the complex mathematical product between the input signal and a complex 2^{nd} local oscillator. The baseband signals were then integrated and ratioed to produce the complex gain measurement. This receiver also included a measurement test sequencer for setting test frequencies, switch states and antenna beam states. The receiver is quite fast, capable of providing 80,000 independent measurements per second. This receiver is currently in use in many antenna test facilities.

Antennas continued to advance during this time period with one interesting development being antennas with direct digital IF outputs. The Panther 6000 was modified to be able to directly accept this high speed digital data from the antenna [4,5].

The design of the next generation receiver combines the lessons of the past with the emerging technologies and technical needs of the future.

3. Next generation receiver design goals

The next generation receiver design was largely driven by the following constraints:

1. The receiver should have predictable and stable operation that can be readily validated. The approach used here is to minimize analog circuitry and include internal performance validation tools. Most of the receiver including the down converters and signal demodulators are implemented in digital form.

2. High quality analog signal measurements require well shielded IF preamplifiers combined with very low jitter analog to digital converters. One of the most difficult aspects of the new receiver development was minimizing coherent leakage between the signal and reference channels. This was accomplished by a combination of shielding, circuit layout, optical isolation and clock edge control. Planar near-field measurements are quite sensitive to coherent leakage which produces spurious on axis energy.

3. Many next generation antennas will require a more thorough characterization, faster measurement speeds and high speed low duty cycle pulsed operation. The new receiver needs to be dynamically reconfigurable on a per measurement basis. Most antenna measurement systems use time division multiple access (TDMA) to sample multiple beams rapidly. In TDMA, the antenna is sequentially switched to various beam states and frequencies. High speed gated TDMA operation with matched filtering maximizes the measurement SNR.

An alternate approach is the use of frequency division multiple access (FDMA) in which multiple beam states are measured simultaneously using different RF or 1^{st} LO frequencies. FDMA supports a larger measurement throughput at equivalent TDMA integration times resulting in a better signal to noise ratio.

4. Improved pulse measurement capabilities are needed. State of the art active antennas can operate at transmit pulse widths less than 1 microsecond. Measurement integrators in the new receiver can be gated with 10 nanosecond resolution as compared to the 3 microsecond resolution of the previous generation receiver. Still higher measurement efficiency can be achieved by rapidly switching between the transmitter and receiver signal integrators at the pulse repetition frequency (PRF).

5. A long product life with a clear evolutionary path is needed. This is achieved by using a scalable and evolvable hardware design based on mainstream technology and components. The receiver hardware uses field programmable gate array (FPGA) technology at the foundation. The FPGA is programmed using the VHDL and Verilog languages. This is combined with a stable long lived ANSII C++ control and signal processing software environment that is operating system and software vendor independent.

6. The basic receiver design and technology should be modifiable and scalable. A modifiable architecture provides operational and product flexibility. A scalable architecture supports the implementation of smaller and larger systems to follow emerging needs.

7. Several new user interface ideas have been explored in this receiver. These include a web based interface, a touch screen interface, an unusual real time LED based “phi” signal display and a connector display to help with receiver cabling.

4. Instrumentation receiver architecture

The receiver hardware includes a high speed test sequencer, IF frequency analog and digital interfaces, a high speed FPGA based digital signal processor and a control computer.

The test sequencer is a specialized computer with an instruction set optimized for antenna beam control. The test sequencer sets the antenna and measurement state for each different measurement. This state vector typically contains test configuration commands such as antenna beam steering or port selection, the RF test frequency, attenuator settings, signal integration times and similar information. The measurement configuration state vectors form a time division multiple access (TDMA) list which is repeated at each measurement location. The measurement list can be quite large with some antenna tests acquiring thousands of separate measurement configurations in a single near-field data acquisition pass.

The measurement test sequencer is implemented as VHDL code within a FPGA. The beam state commands are transmitted via a high speed serial data bus to the rear panel and other optional external I/O modules. The I/O modules typically include a pair of synthesizer control ports and three 8 bit control ports. The entire beam state can be updated in 1.5 microseconds.

The receiver IF inputs can be analog, digital or combined. Analog signals between 8 and 400 MHz are digitized by a highly shielded, high performance analog to digital converter. Digital IF signals from an antenna at rates up to 800 megabytes per second can be processed in real time by the receiver.

An advantage of the new receiver design is that the IF processing is fully implemented in digital form. The core of the receiver is a very high speed FPGA based digital signal processor which is a combination of multiple high speed hardware DSP processors and logic under firmware control. The high speed signal processor has 1 Gbyte of random access memory for data storage.

The FPGA core performs the IF down conversion to baseband, the S21 ratiometric conversion and the measurement signal integration. The digital IF signal is downconverted by forming a complex product with the receiver quadrature local oscillator (LO). The down converted quadrature baseband output is available to various demodulators that can be very rapidly and dynamically selected on a per measurement state basis or even a pulse state basis. For example, a S21 firmware module produces a pulse gated matched filter output corresponding to the complex ratio between the two IF inputs. Other signal processing modules provide statistical measurements, spectral measurements and high resolution pulse profiling using the Hilbert transform methods [1,2,3].

The high speed digital signal processor, other receiver subsystems and the user interface are controlled by a microprocessor running FNX software.

Many antenna test facilities have government security requirements. This receiver has been made compatible with operation in these secure environments by insuring that all nonvolatile writeable memory is removable.

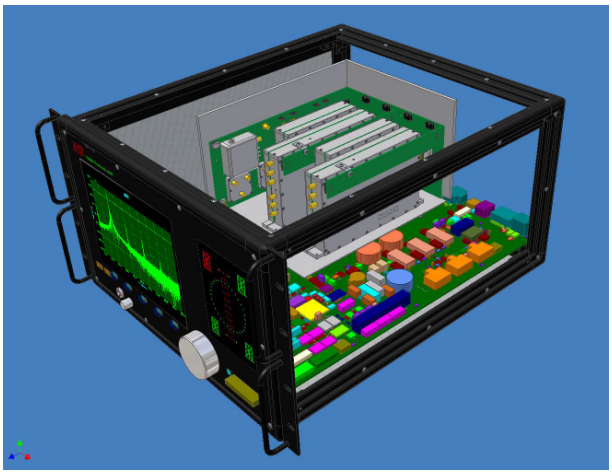

Figure 2 – CAD model showing internal hardware

Figure 2 shows the internal layout of the receiver. The gray boxes are shielded analog I/O modules. The lower main circuit board includes the high speed digital signal processor and microprocessor.

5. Receiver hardware interfaces

Test sequencer interface: The antenna beam state, switch settings, internal receiver configuration and RF / LO synthesizer tuning are all under the control of the beam sequencer. Multiple distributed test sequence controllers are supported using separate 150 megabit per second synchronous serial communication links. This bit rate provides a complete beam state update in 1.5 microseconds. Several additional I/O control lines are available for specialized very high speed test control applications such as pulse and very high speed switch control. These I/O lines can be updated within 10 nanoseconds.

RF / IF interface: The instrumentation receiver can accept various combinations of analog and digital IF inputs. The analog inputs accept IF signals between 8 and 400 MHz. The analog inputs include dynamically switchable IF filters and gain stages. Several different digital IF inputs are available at sample rates up 800 megabytes / second.

Computer interface: This instrumentation receiver interfaces to the outside through a 10/100T Ethernet port. This interface is used for host data transfers, host control and a web browser. Other computer interfaces are possible including USB.

6. Software

The receiver internally uses FNX, a NSI developed software program. This program provides math intensive signal acquisition, simulation, processing and display capabilities. One of the design priorities is a long software life. FNX is operating system independent and is coded in ANSI C++, the industry standard for large software applications.

This software uses a state space object oriented programming foundation combined with an extensive vector math processor and scripting to support real time math intensive signal processing and display operations. Core structures provide general software services for all derived objects including state transition control, interobject communications, fault management and scripting. Measurements, simulated data and processed data are stored equivalently in self describing data container objects.

7. User interface

Several different user interfaces are supported including a web browser interface and an optional LCD touch screen. The web browser interface provides a way to remotely view data and control the receiver. Ajax technology provides real time display updates.

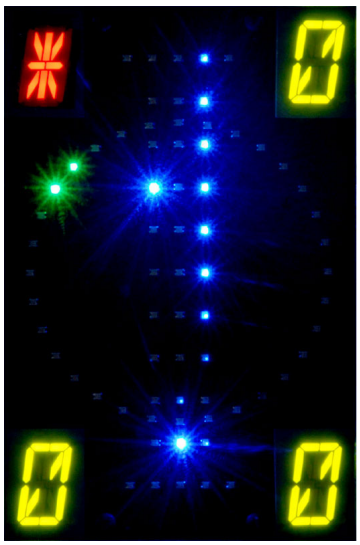

Figure 3 – Phi display

Figure 3 shows the novel "phi display" that is uses a non-uniform array of multicolor LEDs. This reconfigurable display is intended to intuitively show instantaneous signal characteristics and overall receiver performance during setup and test operation. The display is bright, colorful and is designed for very fast dynamic updates. Four 16 segment single character alpha-numeric displays show current trigger and switch state information. A ring of RGB LEDs typically shows RF phase information and the three vertical RGB LED bars show various types of amplitude information. For the specific low SNR example shown in figure 3, the green ring is showing the S21 phase and the 3 vertical blue bars are showing 10, 1 and 0.1 dB S21 signal level steps. The noise causes the right blue bar to elongate vertically with a Gaussian intensity distribution. Additional phi displays can be remotely located and controlled by one of the same high speed serial ports that are used to drive optional external auxiliary antenna test sequencers.

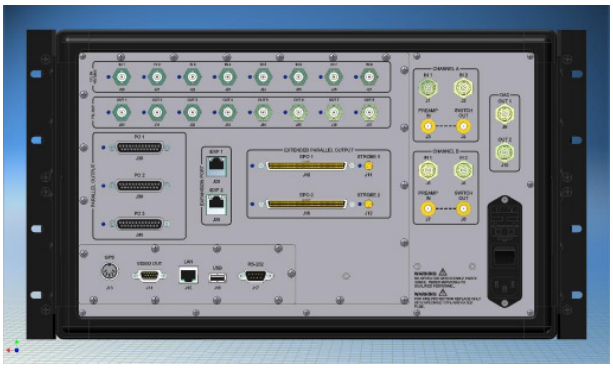

Figure 4 – Receiver rear panel with LED status indicators

Figure 4 shows another specialized user interface which is located on the receiver rear connector panel. Many of the connectors on this panel have adjacent LED indicators which are used to help with cable installation and troubleshooting. One indicator function is used to point out where to connect a cable. A second function uses the indicators to show the logic levels present at the connectors. A third function uses the indicators to support various receiver diagnostic tests.

8. Summary

Rapid advances in antenna technology have required similar advances in the antenna measurement systems. The phase coherent instrumentation receiver directly influences the overall antenna test capabilities, accuracy and speed. The new receiver development described in this paper was influenced both by lessons from the past and the directions of future technology. Emerging instrumentation receiver requirements include faster, more capable and more accurate measurements, digital IF inputs and better pulse measurement capabilities.

9. REFERENCES

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